REMARKS

The enclosed is responsive to the Office Action mailed on July 7, 2004. Applicants have amended claims 1, 4-5, 9, 12, 17, 21-22, 24, and 26; canceled claims 2-3, 13, and 23; and added new claims 31-41. Claims 1, 4-12, 14-22, 24-41 are pending.

Drawings

As identified by the Examiner, the reference to numbers "330(1)...330(j)" in Figure 3 has been corrected to read "350(1)...350(j)." No new matter has been disclosed.

Claim Objections

The Office Action objected to claims 4 and 9 as having the informality of using the word "patter" instead of "pattern." Applicants note that the objection to claim 4 should be instead applied to claim 5 as it contains the informality. Claims 5 and 9 have been amended accordingly.

The Office Action objected to claim 12 as having the informality of using the word "processor" instead of "method." Claim 12 has been amended accordingly.

Claim Rejections – 35 USC § 112

The Office Action rejected claims 8, 20, and 29 under 35 USC § 112 paragraph 1 as failing the written description requirement. Claims 8, 20, and 29 are original claims. As a part of the specification these original claims constitute a disclosure of the subject matter and should not be subject to rejection because the subject matter is lacking in the description. (MPEP 608.01(l).) For at least this reason, Applicant respectfully submits that this rejection has been overcome.

The Office Action rejected claim 14 as having insufficient antecedent basis for the limitation "each execution core" in line 2. Claim 9 has been amended to provide for the proper antecedent basis.

The Office Action rejected claim 21 as having insufficient antecedent basis for the limitation "the first" in line 1 of the claim. Applicant respectfully submits that Claim 21, as amended, finds proper antecedent basis in the language of Claim 17 "a first set of nodes of the execution core."

The Office Action rejected claim 30 as having insufficient antecedent basis for the limitation "the first set of voltage nodes" in line 2. Applicant respectfully submits that Claim 30, as amended, finds proper antecedent basis in the language of Claim 22 "a first and second execution core to operate in FRC mode, each having a set of voltage nodes."

Claim Rejections – 35 USC § 102

The Office Action rejected claim 1 under 35 USC § 102(b) as being anticipated by Bock et al., US Patent No. 5,155,856. Applicants have amended claim 1 to include limitations from claims 2 and 3 and will therefore address the rejection to claim 1 as a part of the following section regarding the 103 rejections of claim 2 and 3 below.

The Office Action rejected claim 9 under 35 USC § 102(b) as being anticipated by Bock et al., US Patent No. 5,155,856. Applicants have amended claim 9 to include limitations from claim 13 and will therefore address the rejection to claim 9 as a part of the following section regarding the 103 rejection of claim 13 below.

The Office Action rejected claim 22 under 35 USC § 102(b) as being anticipated by Bock et al., US Patent No. 5,155,856. Applicants have amended claim 22 to include limitations from claim 23 and will therefore address the rejection to claim 22 as a part of the following section regarding the 103 rejection of claim 23 below.

Claim Rejections – 35 USC § 103

Claims 1-16

Applicants have: 1) amended claim 1 to include at least some of the limitations of claims 2, 3, and 5; and 2) amended claim 9 to include at least some of the limitations of claim 13. The Office Action rejected claims 2, 3, 5, and 13 under 35 USC § 103(a) as being obvious over Bock et al., US Patent No. 5,155,856, and in view of Milburn, US Patent No. 5,758,058. Applicants will address the 103 rejection with respect to amended claims 1 and 9.

The combination of Bock and Milburn does not teach or suggest Applicants' claims 1 and 9 as amended. In claim 1, Applicants are claiming a FRC processor that at least includes "a first and second scan chain to transfer data to one or more nodes of the first and second execution cores" and "a reset module to provide an identical bit pattern to the first and second scan chains." In claim 9, Applicants are claiming "a method for resetting a multicore FRC processor" that at least includes "generating a bit pattern in a reset module of the multicore FRC processor" and "applying the bit pattern to a corresponding scan chain in each of the execution cores of the processor."

In contrast, Bock discloses an external reset module (that is, it is external to the processing unit) for a non-FRC processing unit. The reset control (RC) 20 of Bock is located on the clock chip 6 which is external to the processing unit (PU) 1. (See Bock, Fig. 3 and Col. 3, lines 21-22.) There is no support in Bock to assert that the reset control, which is Bock's analogous reset module, provides the 0 value of reset to the PU. As noted on page 4 of the Office Action, the 0 (for reset) is provided by the AND gate 30. This means that the 0 value provided to the SRLs on reset comes from outside of the reset control.[1,2]

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[1] On normal operation, meaning there is a no reset condition present, the SERIAL DATA INPUT signal 22z provides for the input pattern to the AND gate 30. AND gate 30 then provides the input to the SRLs. (Fig. 4; Col. 6, lines 12-18.)

[2] As the Applicants interpret Bock, Figure 4 depicts the SIF RESET 0 and SIF RESET BIT 1 signals as inputs to AND gates 36a, 36b, and Figure 4 cannot be depicting the PU as those signals are not sent to the PU (see Figure 3 and col. 3, lines 65-67). Figure 4 also does not depict the RESET COND 21 as an input, which Figure 3 shows as an input to the PU.

Milburn describes "a method and apparatus for initializing both processors in a master/checker fault detecting microprocessor." (See Abstract.) Milburn also describes "signaling a microcode routine in both processors. This causes both processors to begin executing their own microcode routines at the same time." (Col. 2, lines 53-55.) As discussed in the background of the present application, the use of microcode initialization requires large and complex reset codes that are very costly to develop, debug, and validate because of the large number of nodes that need to be put into a particular state for a FRC processor.

The combination of Bock's non-FRC external reset module and Milburn's microcode based FRC reset requires modification that is not obvious to one skilled in the art. Specifically, the statement from the Office Action that it is "obvious to include the improved microcode of Milburn to the reset procedure of Bock et al." shows the lack of obviousness of the combination in that: 1) it is not clear how the microcode would trigger an external reset module; and 2) it is not clear whether the external reset module is even used in the combination to provide a bit pattern (in which case this is a code reset implementation different from what is claimed, because what is claimed includes, among other things, an internal "reset module" and a "pattern generator" to drive "scan chains" in two "execution cores"). Thus, the combination fails to make obvious at least the claim limitations of: 1) an "FRC processor" with an internal "reset module" including a "pattern generator" to drive an "identical bit pattern" to "scan chains" of both "execution cores" (see claim 1); and 2) an "FRC processor" with an internal "reset module" "generating a bit pattern" and applying it to "a corresponding scan chain in each of the execution cores" (see claim 9). Additionally, Applicant respectfully submits that the combination of Bock and Milburn relies on hindsight. At the time of Milburn's filing (1996), Bock was already published and known to those skilled in the art (issued in 1992). At the time of Applicants' filing (2001), FRC processors were still reset by code (see Applicant's background).[3] In sum, Applicant respectfully submits that the

[3] It should be noted that Applicant's independent claims should not be construed to exclude the use of reset code in addition to what is claimed.

combination fails to teach or suggest all of the limitations of the claims as amended and relies on hindsight.

As claims 4-8 and 10-12 are dependent on claims 1 and 9, Applicants respectfully submit that the rejections relating to these claims are also successfully traversed for at least the same reasons.

Claims 17-21

The Office Action rejected claim 17 under 35 USC § 103 as being obvious over Colley et al., US Patent No. 4,325,120, in view of Bock et al, US Patent No. 5,155,856. The combination of Colley and Bock does not teach or suggest Applicants' claim 17 as amended. Applicants are claiming "a processor" including "first and second execution cores to be operated in an FRC mode" and including "a reset module to apply a bit pattern to the scan chains of the first and second execution cores."

As discussed above, Bock describes an external reset module (that is, it is external to the processing unit) for a non-FRC processing unit.

Colley describes "indicat[ing] to the execution unit its function in a system employing FRC (functional redundancy checking)." (Col. 166, lines 12-14.) Colley also describes that "two or more execution units are OR-tied for performing FRC functions, with one execution unit designated master and the other(s) designated checker(s)." (Col. 170, lines 11-13.) Colley does not describe resetting a FRC processor.

Similar to the prior rejection, the combination of Bock's non-FRC external reset module and Colley's FRC processor requires modification that is not obvious to one skilled in the art; and thus the combination of Bock and Colley does not provide for all of the elements of the claim. Additionally, Applicant respectfully submits that the combination of Bock and Colley relies on hindsight. At the time of Milburn's filing (1996) Bock was already published and known to those skilled in the art (issued in 1992). At the time of Applicants' filing (2001), FRC processors were still reset by code (see Applicant's

background).[4] In sum, Applicant respectfully submits that the combination fails to teach or suggest all of the limitations of the claims as amended and relies on hindsight.

As claims 18-21 are dependent on claim 17, Applicants respectfully submit that these claims are also in condition for allowance.

Claims 22-30

Applicants have amended claim 22 to include at least some of the limitations of claim 23. The Office Action rejected claim 23 under 35 USC § 103(a) as being obvious over Bock et al., US Patent No. 5,155,856, and view of Colley et al., US Patent No. 4,325,120. Applicants will address the 103 rejection with respect to amended claim 22. The combination of Colley and Bock does not teach or suggest Applicants' claim 22 as amended. Applicants are claiming "a FRC processor" including "a reset module, including a pattern generator, to drive a data signal and a clock signal to the sets of voltage nodes, responsive to occurrence of a reset event, the data signal to place the voltage nodes of the sets in specified logic states."

As discussed above, Bock discloses an external reset module (that is, it is external to the processing unit) for a non-FRC processing unit. Colley discloses that "two or more execution units are OR-tied for performing FRC functions, with one execution unit designated master and the other(s) designated checker(s)." (Col. 170, lines 11-13.) Colley does not disclose resetting a FRC processor.

Similar to the first 103 rejection, the combination of Bock's non-FRC external reset module and Colley's FRC processor requires modification that is not obvious to one skilled in the art; and thus the combination of Bock and Colley does not provide for all of the elements of the claim. Additionally, Applicant respectfully submits that the combination of Bock and Colley relies on hindsight. At the time of Milburn's filing (1996) Bock was already published and known to those skilled in the art (issued in 1992).

[4] It should be noted that Applicant's independent claims should not be construed to exclude the use of reset code in addition to what is claimed.

At the time of Applicants' filing (2001), FRC processors were still reset by code (see Applicant's background).[5] In sum, Applicant respectfully submits that the combination fails to teach or suggest all of the limitations of the claims as amended and relies on hindsight.

As claims 23-30 are dependent on claim 22, Applicants respectfully submit that the rejections relating to these claims are also successfully traversed for at least the same reason.

New Claims

Newly added claims 31-41 add no new subject matter and are in condition for allowance for at least the same reasons as discussed above.

[5] It should be noted that Applicant's independent claims should not be construed to exclude the use of reset code in addition to what is claimed.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance, for which early action is earnestly solicited.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 12/1, 2004

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In the Drawings

The attached drawing sheet contains an amendment to Figure 3. Reference to numbers 330(1)...330(j) has been corrected to read 350(1)...350(j). Applicants submit that no other figure has been amended and no new matter is disclosed.

Attachment(s): Replacement Sheet Figure 3 as Designated in the Top Margin.